Methods measure power electronics' efficiency

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Validating the sytem efficiency of a power-electronics circuit is essential in evaluating the overall system performance, design optimization, and sizing of cooling systems. **Figure 1** shows the conventional method of performing efficiency measurement. The power-electronics system operates at the rated output-power level, and, by measuring the input power and output power, you can calculate the system's efficiency using the **equation** $\eta=(P_{OUT}/P_{IN})\times100\%$, where P_{OUT} is output power and P_{IN} is input power. In other words, the measured input power is equal to the output power plus the power loss of the system.

However, measuring the efficiency of a high-power system that delivers power to loads such as motors, generators, or industrial-computer equipment requires a source that delivers the rated power. The infrastructue therefore should comprise a suitably rated source and an equivalent load that can support the rating of the power-electronics system you are evaluating. These requirements can drive up the facility's infrastructure cost; for one-time design-validation measurements, this cost is difficult to justify.

This Design Idea describes alternative methods of measuring the efficiency of a high-power power-electronics system that simplifies the test-infrastructure requirement by eliminating the test load and using a source that must support only the loss of the power-electronics system. **Figure 2** shows the proposed method, which eliminates the test load by shorting the output/load terminals. The system's control algorithm maintains the required input- and output-current amplitude and frequency by developing circulating reactive power. IGBTs (insulated-gate bipolar transistors) and magnetic components dominate the system's losses, which are functions of the amplitude and frequency of the input and output currents. The loss is also less sensitive to the power-factor and PWM (pulse-width-modulation) index.

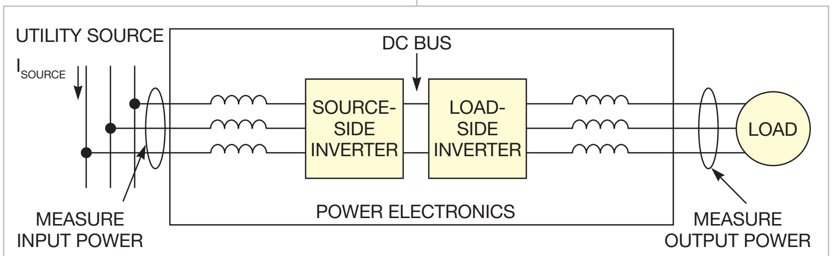

Figure 1 In a conventional method of performing efficiency measurement, the power-electronics system operates at the rated output-power level.

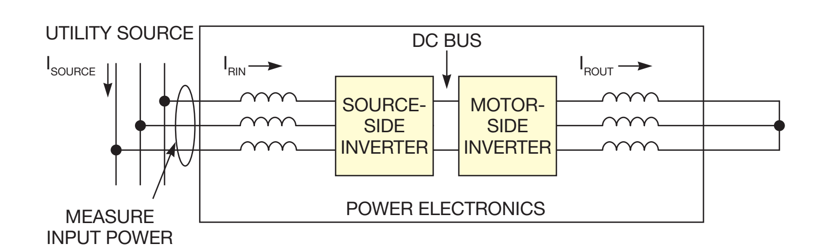

Figure 2 This method eliminates the test load by shorting the output-load terminals.

To know the required input and output current, you must estimate the system's power factor, the motor's back EMF (electromotive force), and the systems's source voltage. This example uses a field-oriented control for both source- and load-side inverters, resulting in the following **equations**:

$$I_{ROUT} = I_{ROUT\_RE}+jI_{ROUT\_IM} = \frac{P_{OUT}}{\sqrt{3}V_{BEMF}};$$

$$I_{RIN} = I_{RIN\_RE}+jI_{RIN\_IM} = \frac{P_{RIN}}{\sqrt{3}V_{GRID}} = \frac{P_{OUT}/\eta_E}{\sqrt{3}V_{GRID}},$$

where I_{ROUT} is the required output current, which comprises real current, I_{ROUT_RE}, and reactive current, I_{ROUT_IM}; I_{RIN} is the required input current, which comprises the real current, I_{IN_RE}, and the reactive current, I_{IN_IM}; P_{RIN} is the

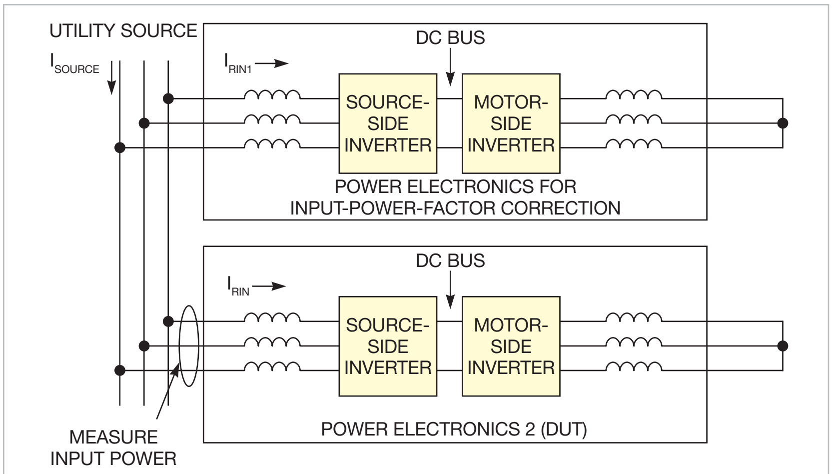

Figure 3 This method uses two identical power-electronics systems. The second system offsets the input reactive current that the test system creates.

required input power; P_{OUT} is the output power at the test condition; V_{BEMF} is the motor's back EMF; V_{GRID} is the grid voltage; and η_E is the estimated efficiency of the circuit.

By maintaining the input current to be I_{RIN} and the output current to be I_{ROUT}, the measured input real power will be close to the power loss, P_{LOSS}, at the actual output-power level, P_{OUT}. Therefore, you can calculate the efficiency as follows: $\eta=(P_{OUT})/(P_{OUT}+P_{LOSS})\times 100\%$.

If the measured efficiency, which you calculate using this **equation**, does not quite match the estimated efficiency, η_E, update the second **equation** using the measured efficiency, η, and repeat the measurement until they are close. Calnetix (www.calnetix.com) has used this method to evaluate the efficiency of a 125-kW power-electronics system, compared the results with the conventional measurements, and found them to be closely matching.

Most high-power power-electronics systems have high efficiency, which means that the real current is much less than the reactive current. To reduce the required current from the grid, you can use the method in **Figure 3**, which uses another identical system to offset the input reactive current that the test system creates. By providing a path for circulating reactive power, the utility sources the lost power only, not the total power. In **Figure 3**, the input current of the second power-electronics circuit is $I_{RIN}=I_{RIN\_RE}+jI_{RIN\_IM}$. By setting the first circuit to have an input current of $I_{RIN1}\approx I_{RIN\_RE}-jI_{RIN\_IM}$, the power from the source is only $I_{SOURCE}=I_{RIN1}+I_{RIN}\approx I_{RIN\_RE}+I_{RIN\_RE}+j(I_{RIN\_IM}-I_{RIN\_IM})=2I_{RIN\_RE}$. The circuit uses the input current from the source only to overcome the power losses of the two circuits, thereby eliminating the need for a high-power infrastructure.EDN

Circuit extends battery life

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Two previous Design Ideas describe simple ways to automatically disconnect a battery from its load after a preset on period, which extends battery life (**references 1** and **2**). These circuits have little loss in standby operation, but they do draw some current. The circuit in this Design Idea presents a simpler way to perform the same function with fewer components and with no power consumption during standby operation (**Figure 1**). Moreover, the network comprising R_2, D_2, and C_2 activates and deactivates the circuit. An additional control signal, control on/off, becomes slower than the battery's on/off cycle.

Switching S_1 to Position 1, the on position, the 24V battery quickly charges capacitor C_1 through diode D_1. That voltage drives transistor Q_1 into saturation. Q_1's saturation magnetizes and activates relay coil L_1, connecting the battery to the main power and control board. Meanwhile, capacitor C_2 charges more slowly through 100-kΩ resistor R_2, thus generating the control on/off signal with some delay relative to the relay coil's closing. That scenario occurs after

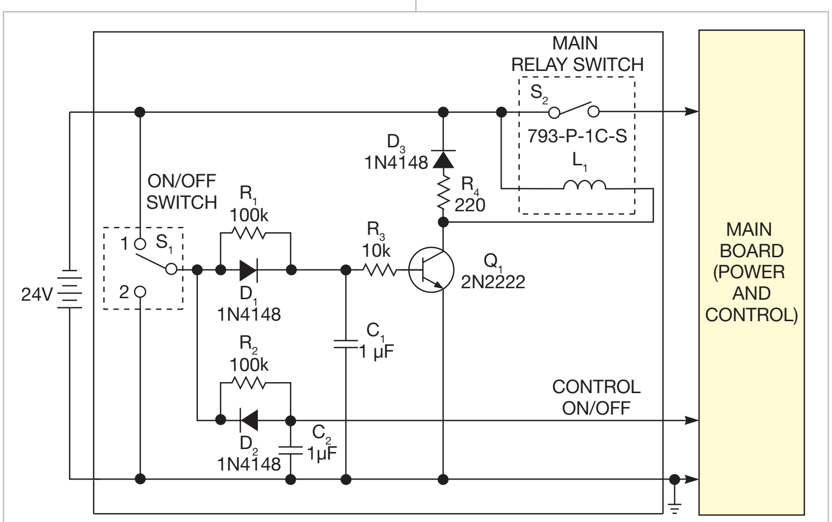

Figure 1 This on/off management circuit uses a relay to remove battery power.

the proper power supply to the power stage and control circuits.

Switching S_1 to Position 2, the off position, causes capacitor C_1 to slowly discharge through resistor R_1 when diode D_1 is off. That action delays Q_1's turn-off. Before Q_1 turns off, C_2 quickly discharges through D_2, indicating that the control should shut down the power. The relay switches off with minimum current. Once Q_1 is off, the relay coil demagnetizes through R_4 and D_3. The relay switches off, disconnecting the main power and control board from the battery. During this off state, current flows neither in the on/off circuit of the management board nor to the main board.EDN

REFERENCES

1 Gimenez, Miguel, "Scheme provides automatic power-off for batteries," *EDN*, May 13, 2004, pg 92, http://bit.ly/aUdD3s.

2 Xia, Yongping, "Battery automatic power-off has simpler design," *EDN*, March 31, 2005, pg 80, http://bit.ly/bLJNgb.

Pulse generator corrects itself

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Using a shift register with parallel output is a common way to design a pulse generator with N inputs and pulsed outputs having a width of T/N. To keep the output pulses consecutive, you can use feedback from the last output to the first input. At power-on, such a circuit can have a random combination of logic zeros and ones, forming an undesired data content of the shift register. To avoid circulating undesired states and to enter a proper sequence, you need a special feedback.

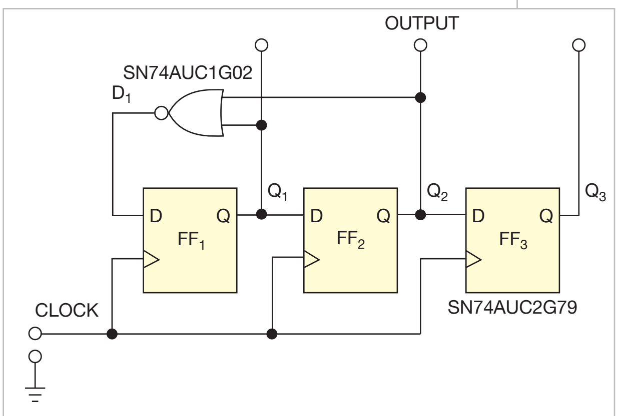

Figure 1 This one-of-three pulse generator uses three ICs, yet it avoids false logic states.

The circuit in **Figure 1** is a three-stage shift register that uses D-type flip-flops. It has three outputs, Q_1, Q_2, and Q_3, each of which produces a periodic pulse having a width of $T_{REP}/3$. $T_{REP}=3T_{CLK}$ is the period at which the sequence repeats at any of the three outputs. A two-input NOR gate creates the feedback. The gate's D_1 output connects to the D input of flip-flop FF_1, and its inputs connect to Q_1 and Q_2. A logic-one bit at D_1 means that, at the nearest low-to-high transition of the clock, this signal will place a logic one at output Q_1.

You can interpret this feedback in words by writing a logic zero into FF_1 at the nearest low-to-high transition of the clock signal, if at least one of the Q_1 or Q_2 outputs has a logic-one state. You write a logic one into FF_1 if both the Q_1 and the Q_2 outputs are at logic zero. This feedback adds a self-correcting feature, which is illustrated by the assumption that the initial state of the circuit is intentionally undesired.

Using this result, the following sequences illustrate state correction, in which the logical states in the bit triads correspond left to right to Q_1, Q_2, and Q_3:

111→011→001→100→010→001
000→100→010→001

From this example, you can see that erroneous state 111 self-corrects within two periods of the clock. For the undesired 000 state, the proper cycling enters at the nearest low-to-high transition of the clock signal.

You can determine the upper limit of the clock frequency from an assumption of the gate output, which changes after a low-to-high transition of the clock. This condition must be ready with a setup time, T_{SETUP}, the next time the clock transitions from low to high (**Figure 2**). Thus, $T_{CLKMIN}=T_{PQHL}+T_{PGLH}+T_{SETUP}$, where T_{PQHL} and T_{PGLH} are signal-propagation delays of the flip-flop and the gate, respectively, at the respective output-level transition. By using the worst-case values of propagation delays from the devices' data sheets, you get a minimum clock period of 4.4 nsec for a supply voltage of 1.8V and a minimum clock period of 3.5 nsec for a supply voltage of 2.5V. As the 3.5-nsec value gives a clock frequency higher than the guaranteed toggle frequency for the flip-flop, you should accept the maximum clock frequency at 275 MHz for a supply voltage of 2.5V. For a supply voltage of 1.8V, the maximum clock frequency should be 227 MHz. The maximum repetition rate of signals at Q_1, Q_2, and Q_3 outputs is the maximum clock frequency divided by three, or 75.6 MHz.EDN

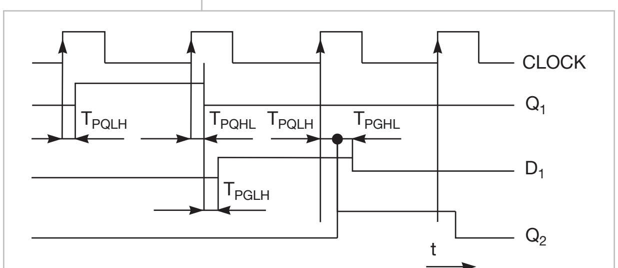

Figure 2 The circuit generates glitch-free logic waveforms that are successive in time and have accurate duty cycles of 33.3%.

Reflective object sensor works in bright areas

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When using a reflective object sensor, counting and identifying objects is sometimes difficult in the presence of electrical noise or bright ambient light. The circuit in **Figure 1** shows an inexpensive solution to this problem using three independent and simultaneously working reflective object sensors. The circuit is suitable for many types of objects, but it targets use with objects such as cards.

The circuit uses three OPB704 reflective optical sensors with Schmitt-trigger NAND comparators IC_{1A}, IC_{1B}, and IC_{1C} on each output. IC_{1D} functions as a clock generator, and counter IC_{6B} functions as a divide-by-eight counter that divides the clock frequency. That signal drives IC_{4D}, which acts as a buffer to drive transistor Q_1.

To understand how the circuit works, consider Sensor 2. IC_{1B}'s output will be low if the sensor's phototransistor doesn't detect IR rays reflected from an object. Both of IC_{1B}'s inputs are high; therefore, the D1 input of IC_2 is low. In any case, if the sensor's phototransistor detects IR rays reflected from an object, the D1 input of IC_2 is high. The level corresponding to the current situation transfers through IC_2's Q_1 output (Pin 7) by a write signal on the C input (Pin 9). The write signal is a leading edge of puls-

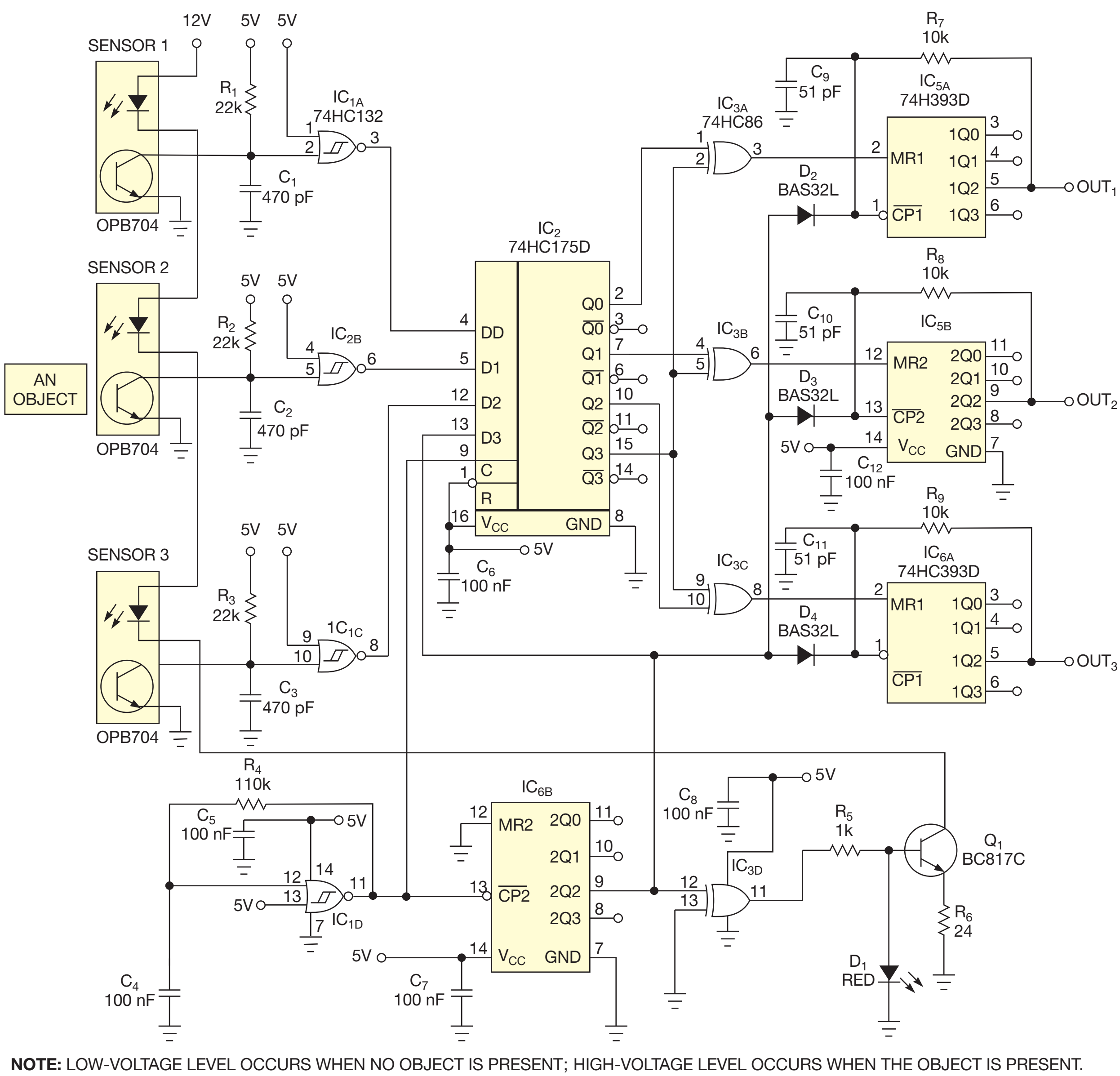

Figure 1 Infrared sensors and logic circuits detect the presence of an object.

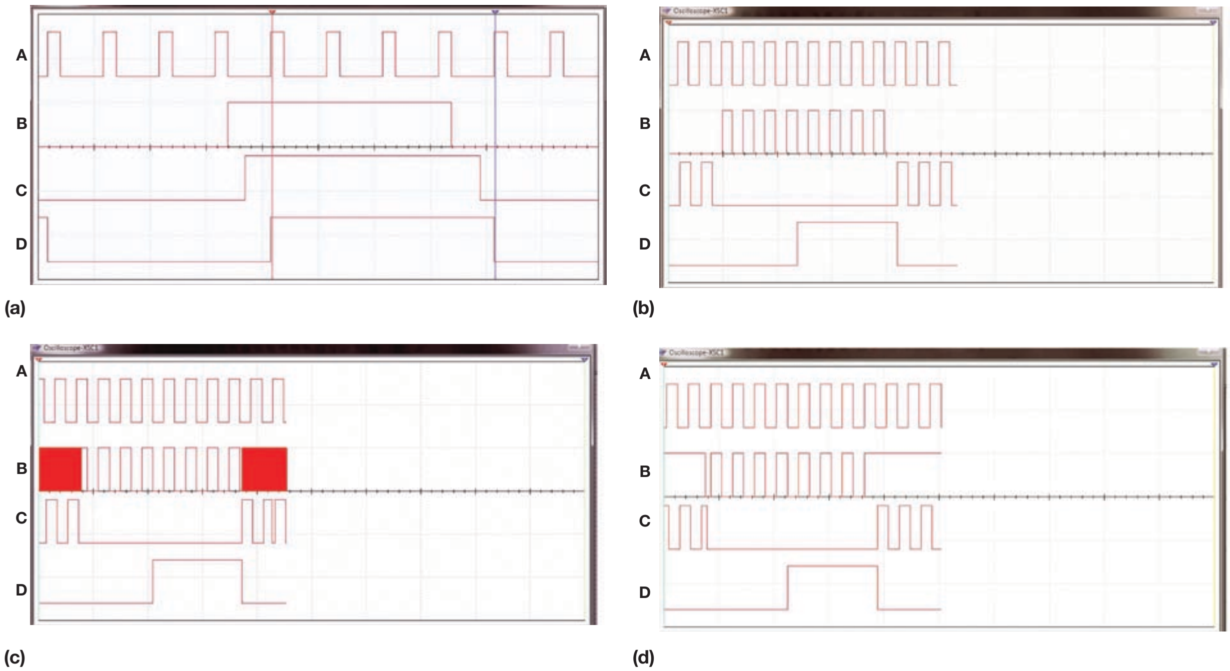

Figure 2 Traces show the process of normalization (a) and three cases of using the presented device (b, c, and d).

es from the clock generator. The signal from divider IC_{6B} becomes the D3 input of IC_2. A level of the divided clock signal transfers to IC_2's Q3 output (Pin 15) upon receiving a write signal from the C input (Pin 9). The signals on the Q1 and Q3 outputs have equal duration except when the sensor's phototransistor detects IR rays reflected from an object. **Figure 2a** shows the process of this normalization. Exclusive-OR gate IC_{3B} compares the Q1 and Q3 outputs from IC_2. If they have the same logic level and duration, then IC_{3B}'s Pin 6 is low, and IC_{3B} generates pulse signals. If signals from outputs Q1 and Q3 on IC_2 are unequal, you must reset counter IC_{5B}'s reset signal, and its output 2Q2 at OUT_2 is low. The Q2 outputs of counters IC_{5A}, IC_{5B}, and IC_{6A} are low whenever the input signals of comparator circuits IC_{3A}, IC_{3B}, and IC_{3C} are unequal. This situation occurs if Sensor 2 doesn't detect an object or receive any external signals—for example, IR noise from fluorescent lamps or interfering ambient light, alternating light, or flashes.

The outputs of IC_{3A}, IC_{3B}, and IC_{3C} are equal only when all phototransistors detect a signal from their respective IR emitting diodes—that is, when a card is presented in front of Sensor 2 (**Figure 2b**). You must choose a clock frequency with regard to a delay time of the system. A leading edge triggers IC_2, a 74HC175, and a falling edge triggers IC_{6B}, a 74HC393. Because of the counters, this system automatically adjusts itself after any changes of frequency in its clock generator. Thus, if counter IC_{5B} does not have a reset signal during a period equal to four periods of a reference signal, its output (Pin 9) is high, and the counter latches through R_8. The logic-high level appears on OUT_2 until you remove the card. In this case, the detected inequality signal from the sensor with the reference signal and the counter, IC_{5B}, causes a reset signal. **Figures 2b**, **2c**, and **2d** show three cases of using the presented device.

Figure 2b shows a case of normal operation. You can see the results of comparing a reference signal (Trace C) and a signal of IC_{1B}'s output (Trace D). The signal of IC_{1B}'s output (Trace B) is low when no card appears. When the card enters the zone of vision of a sensor (Trace B), it is a sequence of normalized pulses. The output of the device at Pin 9 of IC_{5B} (Trace D) changes its level from low to high after four cycles of both signals, but it will immediately change to low if you remove the card.

Figure 2c shows operation of the device under strong IR noise. The signal of IC_{1B}'s output (Trace B) contains some high-frequency signals if a card isn't present and is a sequence of normalized pulses when a card is present. The output of the device at Pin 9 of IC_{5B} (Trace D) indicates the presence of a card by changing its level from low to high after four cycles of these signals. It immediately changes to low if you remove the card from the zone.

Figure 2d shows operation of the device under ambient direct lighting. You can see the results of comparing signals. In this case, the signal at IC_{1B}'s output (Trace B) is constant high when a card isn't present. When the card enters a sensor's zone of vision (Trace B), the signal is a sequence of normalized pulses. The output of the device at Pin 9 of IC_{5B} (Trace D) indicates this condition by changing its level from low to high after four cycles of both signals. It immediately changes from high to low when you remove the card from the zone.

Capacitors C_1, C_2, and C_3 are optional. They protect input circuits from electromagnetic noise when, for example, long wires connect the sensors and the device. Capacitors C_9, C_{10}, and C_{11} provide performance reliability by protecting the counters from short pulses.EDN