Control of a Three-phase Four-wire Inverter

Liping Zheng and Dong Le
Calnetix Technologies LLC
Cerritos, CA, USA
lzheng@calnetix.com and dle@calnetix.com

***Abstract*— In this paper a three-phase four-leg voltage source inverter operating in island mode is described. The four-leg inverter is implemented by using a delta/wye or ZigZag transformer to meet isolation requirement. The control scheme includes an inner current loop providing the capability of fast current limiting and outer voltage loop. Digital sliding mode control is used for the inner current loop which requires higher bandwidth. The voltage loop is implemented in synchronous frame with selected harmonics cancellation for both positive and negative sequence components. Simulation and test of a 125 kW inverter at various operation conditions are presented to verify the validity of the control method.**

***Index Terms*—Three-phase, Island mode, Harmonics cancellation, Current control, Voltage control, Uninterruptible power systems, Pulse width modulation, Inverters, Synchronous frame, Stationary frame.**

I. Introduction

There have been increasing demand for ac power supplies or uninterruptible power supplies (UPS) having low voltage distortion. The voltage distortion which is mainly caused by nonlinear and unbalanced loads will lead to load failures and reduced reliability of the inverter. Therefore, some standards specify the harmonics distortion requirement for the inverters. The international Electrotechnical Commission (IEC) 62040-3 recommends that the total harmonics distortion (THD) of sinusoidal output voltages shall be less than 8 % [1]. It also specifies the maximum distortion of the individual harmonics. There are lots of literatures talking about the different control schemes to reduce THD. However, it is still challenging to have low THD at nonlinear and unbalanced condition since in conventional control, the voltage loop bandwidth is too low to compensate for harmonics frequencies.

Because of the high bandwidth requirements of the voltage loop, even some high-performance feedback control schemes, such as deadbeat control [2]-[5], sliding-mode control [6]-[7], can still have high THD at nonlinear and unbalanced load conditions, although they have very good transient performance under large-signal disturbances. To overcome that, other control schemes have been developed, such as internal model based controller [8], optimal control [9], and repetitive control [10]-[11]. Repetitive control has shown promising results in tracking and rejecting periodic signals. Synchronous frame and stationary frame harmonics cancellation are also widely used to reduce THD when in nonlinear load conditions [12]-[15].

In this design, we describe a new control scheme which use digital sliding mode control (DSMC) for the current loop control in order to have fast current limiting capability which is very crucial when the inverter is running in island mode. The voltage loop is implemented in synchronous frame with selected harmonics cancellation for both positive and negative sequence components. The control scheme is very robust to parameter variation and also is easy to be implemented. A 125kW, 480V inverter has been built to verify the control performance. The simulation and test results show very promising performance.

II. Topology and Control Scheme

The simplified circuit topology of the developed three-phase four-wire island mode inverter is shown in Fig. 1, where V_A is the inverter stage pulse width modulation (PWM) output voltage, I_A is the PWM output current, I_L is the load current in the transformer primary side, V_C is the voltage in the transformer primary side, and V_L is the transformer voltage in the secondary side. The isolation transformer which provides three-wire to four-wire conversion can be delta/wye or ZigZag transformer depending on the applications.

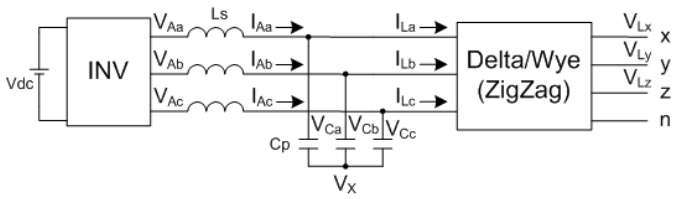

Fig. 1. Simplified circuit topology of the inverter in island mode operation.

The block diagram of the simplified control scheme is shown in Fig. 2. Due to the large current ripple of the PWM output currents, especially at light load condition, two samples synchronized to each PWM cycle is implemented to reduce the switching harmonics of the sampled current signals.

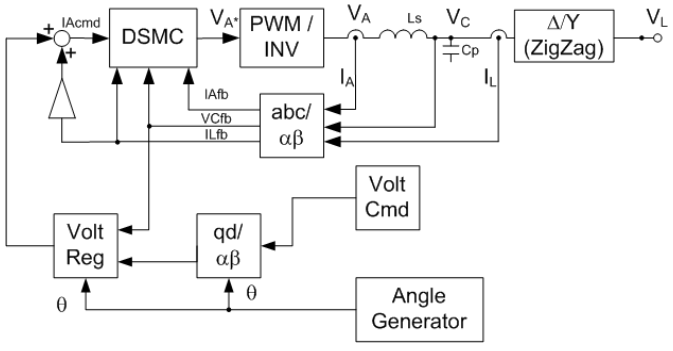

Fig. 2. Simplified control schematic.

Besides of providing isolation, the Delta/Wye or ZigZag transformer also help to reduce certain order of harmonics. The zero-sequence current is also eliminated in the transformer primary side because of three-wire to four-wire conversion of the transformer. Therefore, after using Clarke's transformation to transform variables from stationary *abc* frame into stationary $\alpha\beta$ frame using equation 1, only α-axis and β-axis variables are required to be controlled.

$$[f_{\alpha\beta 0}] = [T_{\alpha\beta 0}][f_{abc}] \tag{1}$$

where variable f can be currents, voltages, and the transformation matrix is given by

$$T_{\alpha\beta 0} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2}$$

Digital sliding mode control (DSMC) is used for inner current loop control [16]-[17]. By using inner current loop, the inverter can have the capability of fast current limiting. The DSMC current control loop is implemented in stationary $\alpha\beta$ frame since current loop has much higher bandwidth than voltage loop so higher order harmonics can also be controlled in stationary $\alpha\beta$ frame. Assuming the load current as disturbances, the current loop subsystem can be written in state space form as

$$\dot{\vec{x}} = A\vec{x} + B\vec{u} + E\vec{d} \tag{3}$$

where the states are

$$\vec{x} = \begin{bmatrix} V_{Cqs} \\ V_{Cds} \\ I_{Pqs} \\ I_{Pds} \end{bmatrix}, \vec{u} = \begin{bmatrix} V_{Pqs} \\ V_{Pds} \end{bmatrix}, \text{ and } \vec{d} = \begin{bmatrix} I_{Lqs} \\ I_{Lds} \end{bmatrix} \tag{4}$$

And the coefficients are

$$\vec{A} = \begin{bmatrix} 0 & 0 & \frac{1}{C_p} & 0 \\ 0 & 0 & 0 & \frac{1}{C_p} \\ -\frac{1}{L_s} & 0 & 0 & 0 \\ 0 & -\frac{1}{L_s} & 0 & 0 \end{bmatrix} \tag{5}$$

$$B = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L_s} & 0 \\ 0 & \frac{1}{L_s} \end{bmatrix} \tag{6}$$

$$E = \begin{bmatrix} -\frac{1}{C_p} & 0 \\ 0 & -\frac{1}{C_p} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{7}$$

The sliding mode surface of the DSMC is chosen as $\vec{s}(k) = C\vec{x}(k) - \vec{I}_{cmdqd}(k)$, and $C\vec{x}(k) = \vec{I}_{fbqd}(k)$. The equivalent control input of the sliding mode control can then be derived as [16]:

$$\vec{u}_{eq}(k) = (CB^*)^{-1}(I_{cmdqd}(k) - CA^*\vec{x}(k) - CE^*\vec{d}(k)) \tag{8}$$

where A^*, B^* and E^* are the discrete forms of the coefficient matrices A, B, and E.

The voltage loop is implemented in synchronous frame with selected harmonics cancellation for both positive and negative sequence components [14]. The simplified voltage regulation block is shown in Fig. 3. The stationary frame voltage error which comes from condenser reference voltage *VCref* and feedback voltage *VCfb* is multiplied by the proportional gain (*Kp*) to create proportional inverter current command which is used to provide fast transient response to the load change.

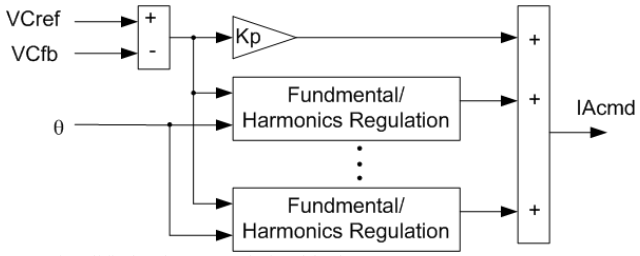

Fig. 3. Simplified voltage regulation block.

The load current harmonics are normally slowly varying, so the harmonics regulations for individual selected frequencies (for example, fundamental, 3rd, 5th and 7th) are implementation in synchronous frame. The advantage of implementing the harmonics regulation in *dq* frame is that the control variables are dc components which are easy to control and monitor. The output of each harmonics regulators are added together to create the integral portion of inverter current command. Anti-windup technique and the amplitude limiting for each harmonics regulation output should be used to avoid the overflow of the control current command. A feed forward signal proportional to the load current is also added to the command current in order to provide fast dynamic response to the load change.

Fig. 4 shows the control scheme where gain *h* is the order of harmonics. Similar function block for the fundamental and harmonics regulations can be used. Positive sequence regulation and negative sequence regulations are both implemented in synchronous frame with integral (*I*) controller only as shown in Fig. 5. The stationary frame voltage error is first converted in synchronous frame. Then integral controller is used on the synchronous frame voltage error. After that, the synchronous frame current command is transformed back to stationary frame.

An angle offset corresponding to the time of about one to two PWM cycles should be added to compensate the system delay which is important for the compensation of higher order of harmonics. The main disadvantage of using many

harmonics compensators in the control is the computational complexity related to transformation and control for each harmonics. Therefore, a fast processor may be required.

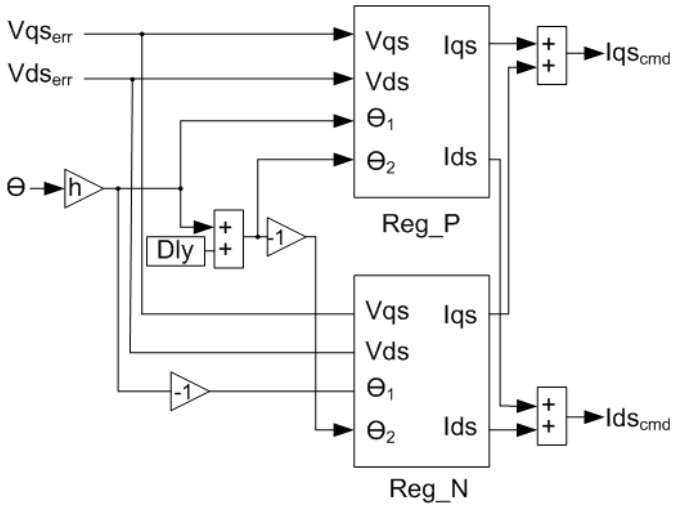

Fig. 4. Control scheme for selected harmonics.

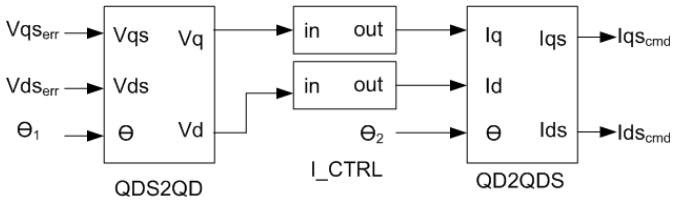

Fig. 5. Integral controller of the voltage in synchronous frame.

III. Simulation and Test Results

A 125 kW, 480V, 150A inverter based on DSP 320F2812 has been implemented to verify the validation of the proposed control scheme. Fig.6 shows the picture of the 125 kW inverter test setup. The output filter inductor value is 250 μH, and capacitor value is 270 μF. The switching frequency is 7500 Hz.

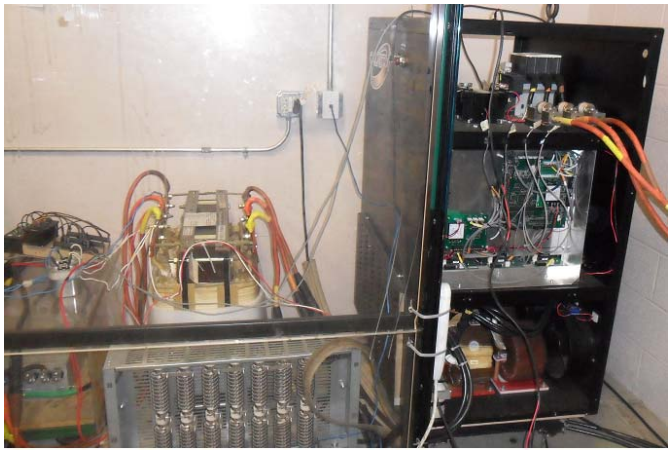

Fig. 6. Picture of the 125kW inverter test setup.

Fig. 7-Fig. 10 show the analyzed current loop and voltage loop transfer functions. The bandwidth of the current loop is about 2 kHz. The voltage loop has large gains at selected harmonics frequencies.

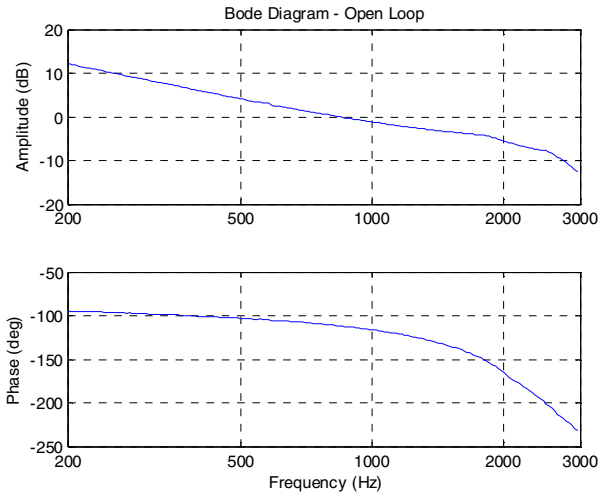

Fig. 7. Open loop transfer function of the current loop.

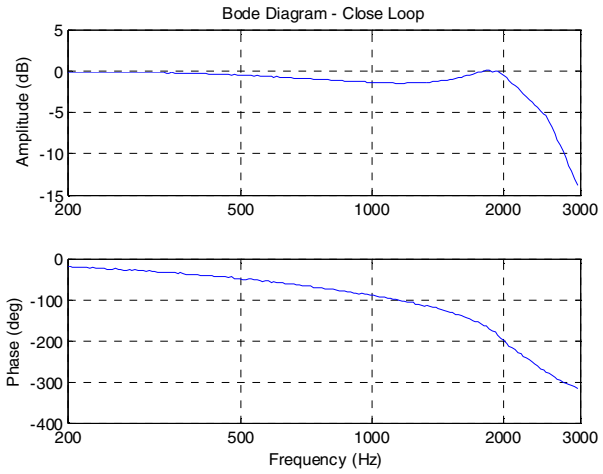

Figure 8. Close loop transfer function of the current loop.

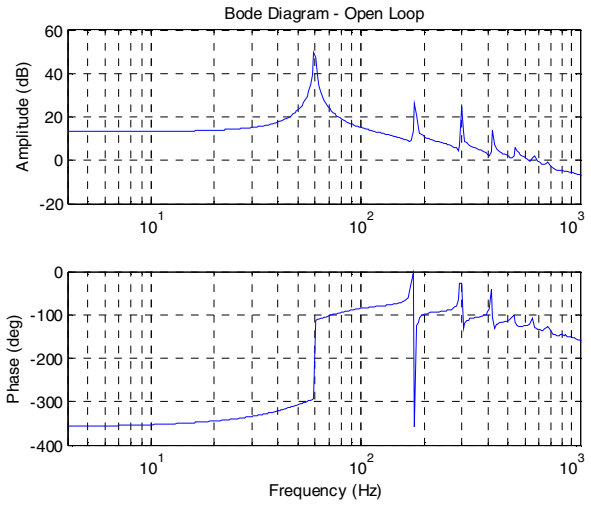

Figure 9. Open loop transfer function of the voltage loop.

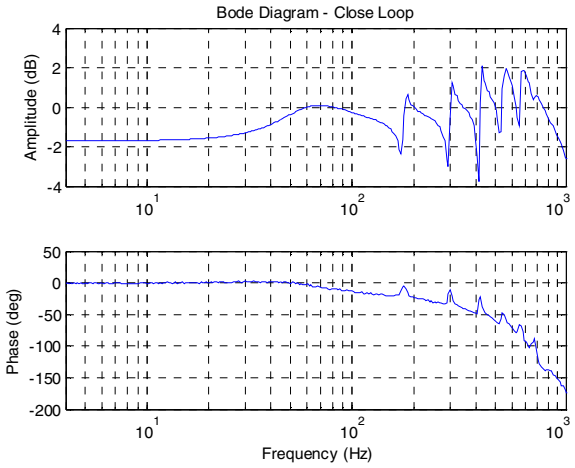

Fig. 10. Close loop transfer function of the voltage loop.

Fig. 11 and Fig. 12 show the simulation results at nonlinear load and unbalanced load conditions. The results show that the proposed controller has very good performance even at nonlinear and unbalanced load conditions.

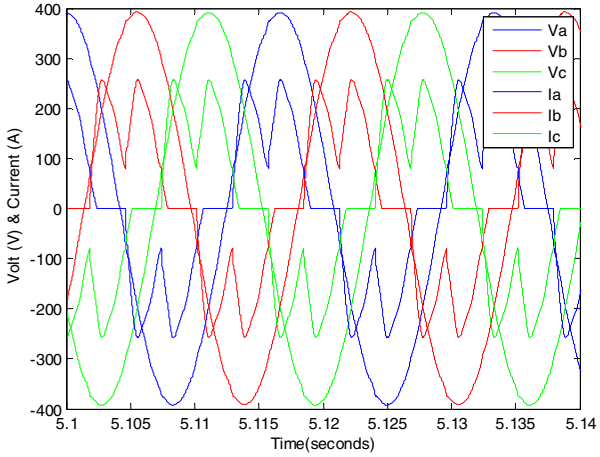

Fig. 11. Nonlinear load performance (3-single phase rectify with the load of 3Ω, 4700uF). The voltage THD is 0.77%.

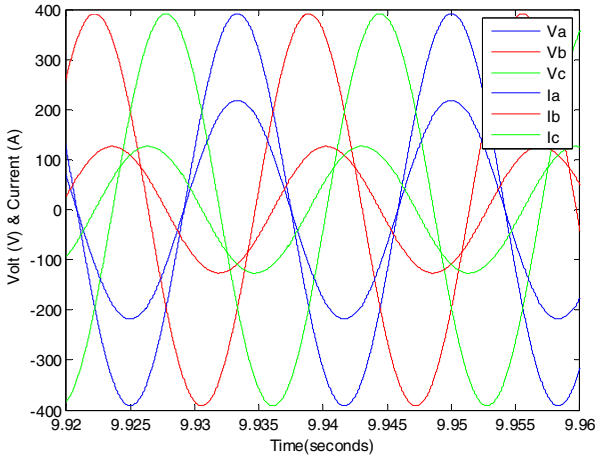

Fig. 12. Unbalance load performance (three-phase voltage unbalance is less than 1%).

Fig. 13 shows the experimental result at active load condition. The switching frequency of the three-phase active rectifier load is also 7500 Hz. The result shows the voltage output is still stable at active load condition. However, it is worth to mention that because of active load especially with the switching frequency is very close to that of the inverter, sub-harmonics may be created which will make the control unstable as shown in Fig. 14 in which the voltage loop gain has been intentionally made very low at low frequency and also the load feed forward has been reduced.

Fig. 15 shows the experimental result at non-linear condition when the output voltage is saturated due to not enough dc bus voltage. Because of the implementation of the anti-windup technique and the amplitude limiting for each harmonics regulation output, when the output voltage is saturated, the output voltage THD will increase but the control can still be stable.

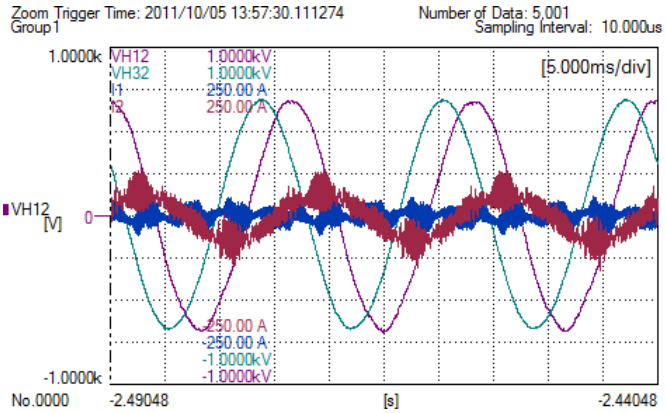

Fig. 13. Measured waveforms at active load condition. (same switching frequency).

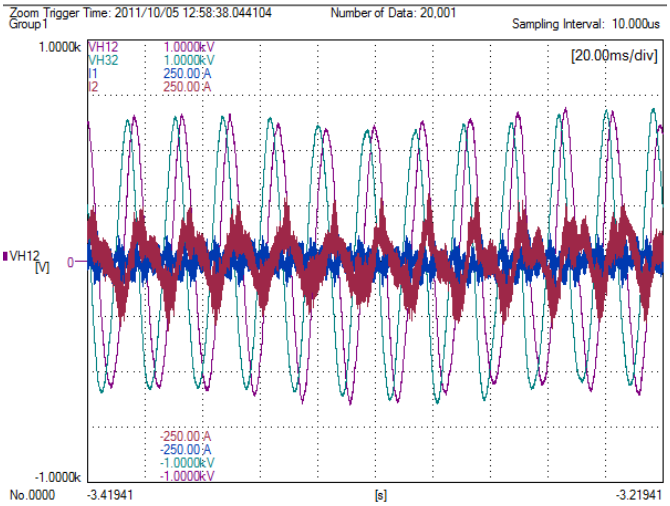

Fig. 14. Measured voltage and current waveforms at active load condition when the proportional gain feed forward gain are very low.

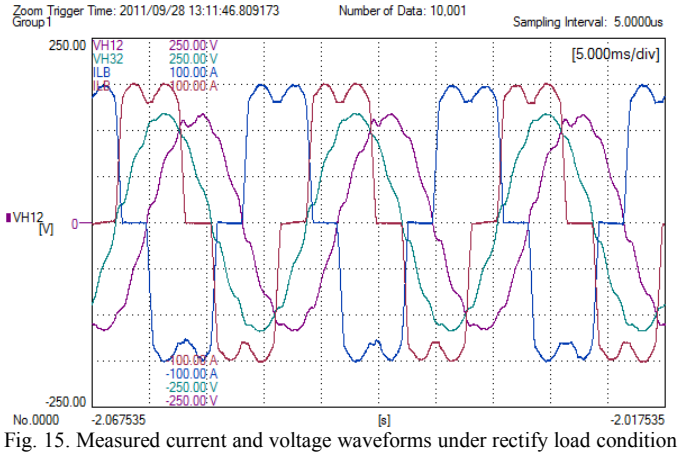

Fig. 15. Measured current and voltage waveforms under rectify load condition with output voltage saturation.

IV. Conclusion

This paper has described the design of a three-phase four-leg voltage source inverter operating in island mode. An isolation transformer is used to provide isolation and four-wire output. The inner current loop uses high performance DSMC. The voltage loop is implemented in synchronous frame with selected harmonics cancellation for both positive and negative sequence components. The simulation and experimental results of a 125 kW inverter at various operation conditions are presented to verify the validity of the control method.

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